SO-DIMM Module — Unbuffered SDRAM/SGRAM Graphics

64-bit (Non-ECC/Parity)
144-pin Module

Revision 0.91

February 1998

Order Number: Not Applicable



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Revision 0.91

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Revision History

Rev.	Description	Date
0.91	• Added clarification to address translation table on page 9	12/1997
0.9	• Update block diagrams on Pages 11-14 to include 512Kx32 devices • Added address translation table for 256Kx32 and 512Kx32 devices • Removed Electrical Timings (Refer to Intel “PC SGRAM” Specification for AC Timing requirements	12/1997
0.2	• Changed the functionality of strapping resistor DQ31 from Memory Timing to CAS Latency (page 15). • Removed CAS latency 4 support. • Remove support for TSOP packages. • Changed the Output Valid from Clock (Tac) from 7.5 nS to 7.0 nS (page 30-31).	5/14/97
0.1	• Clarified memory organization explanation in the sectioned titled, Graphics SO-DIMM Block Diagram (page 10-17). • Removed resistor pull-down from SDA signal when the SPD EEPROM is not present from the section titled, Serial Presence Detect EEPROM. The SPD presence can be determined by sending the I2C address and determining whether an ACK is returned (page 19). • Added an SPD EEPROM address line to pin 62 of the connector in the section titled, Pin Assignments, the section titled, Graphics SO-DIMM Block Diagram, and the section titled, Appendix A - PCB Layout. This allows two modules to be independently addressed (page 9-17, 44-47).	1/16/97
0.09	• Added section titled, Labeling (page 7). • Corrected diagram titled, Pin Assignments to change duplicated pins 116 and 118 to 98 and 100, respectively (page 9). • Added resistor value of 0 ohms to CLK0 and CLK1 series termination in the section titled, Graphics SO-DIMM Block Diagram (page 10). • Changed all references from V_{DD} to Vcc (pages 11-18, 28, 29). • Included a definition of logic-low and logic-high in the section titled, Resistor Strapping Options. Also include strapping resistor value of 4.7K (page 19). • Removed support for two modules from the section titled, Electrical Characteristics (page 20). • Changed the minimum module impedance requirements from 55 ohms to 50 ohms in the section titled, Electrical Characteristics (page 20). • Added suggested flight time data to the section titled, Electrical Characteristics (page 20-24). • Added chip select routing to the section titled, Clock Routing (page 26). • Added total length parameter to sections titled Clock Routing and Chip Selects, Address/Control Routing, and Data Routing (page 26-28). • Changed the maximum timing for two parameters (b and c) from 45 pS to 75 pS in the section titled Data Routing (page 28). • Added statement allowing a 125 pS stub (d) for the strapping resistor (page 28). • Changed the Input Hold Time (Thi) from 1.5 nS and TBD to 1.0 nS (page 18, 31-36, 40-42). • Changed the Output Hold from Clock (Toh) from 1.0, 1.5 nS, 2.0 nS, or TBD to 2.5 nS (page 18, 31-42). • Correct diagram titled, Output Measurement Load Circuit to set reference level from 1.5V to 1.4V (page 43). • Added section titled, Appendix A - PCB Layout (page 44-47).	1/15/97

Rev.	Description	Date
0.08	• Removed most of the resistor strapping options. Only the memory clock option is preserved (page 16, 17). • Added support for TQFP packages (page 6, 18). • Corrected address lines in sectioned titled, *Graphics SO-DIMM Block Diagram* (page 8-15). • Changed the rated capacitance load from 50 pf to 30 pf (page 16, 24-36). • Changed the transition voltage from 1.5 V to 1.4 V (page 16, 24-36). • Added four new parameters (*c+e*, *c+f*, *d+g*, and *d+h*) to the flight time table (page 20).	12/2/96
0.07	• Added the section titled, *Electrical Characteristics* (page 20). • Added the section titled, *PCB Layout Considerations* (page 21-24). • Modified the *Graphics SO-DIMM Block Diagram* section to add resistors to some of the address and control lines. These were based on simulations performed by Intel (page 9, 12, 13, 15).	11/25/96
0.06	• Added the section titled, *Revision History.* • Rotated one of the PQFP SGRAM components 180º to optimize address bus routing on the memory module. This was based on electrical simulation performed by Intel (page 6). • Moved the address bus in the Pin Assignments. This was based on electrical simulations performed by Intel (page 7).	10/7/96
0.05	• Added thickness dimension to section titled, *Mechanical Outline* (page 5). • Mirrored all of the data lines to make them conform better with existing graphic controllers (page 6). • Added the section titled, *Graphics SO-DIMM Block Diagram* (page7-14). • Changed the resistor pull-up/pull-down from 2.2K to 4.7K (page 16). • Modified the resistor strapping option to remove the Memory Size option (6 resistors). Three of these resistors were allocated to Memory Type to allow for additional memory configurations. The remaining three were reserved for future use (page 17).	
0.04-0.05	• Internal Review	9/25/96
0.03	• Shifted the resistor strapping values by one-bit. Previously the resistor options started at DQ28; now it begins at DQ29 (page 7-9).	9/6/96

1.0 Unbuffered Graphics SO-DIMM Module

1.1 General Features

- 144-pin, small-outline, dual-in-line memory module (SO-DIMM).
- 64-bit data bus (non-ECC/Parity)
- Maximum of 8MB per module with extensions to 32MB
- SDRAM/SGRAM
- Single, 3.3V ±10% power supply
- LVTTL-compatible inputs and outputs
- Specification currently defines four module frequencies (speeds); 66 MHz (15 nS), 83 MHz (12 nS), 100 MHz (10 nS), and 125 MHz (8 nS).

1.2 Labeling

Four module frequencies are currently defined; they are:

- 66 MHz (15 nS).
- 83 MHz (12 nS).
- 100 MHz (10 nS).
- 125 MHz (8 nS).

For consistency, modules should be clearly marked indicating their rated frequency in MHz. The speed, in nano-seconds, is optional. This label should be consistent with the module speed setting used in the resistor strapping option.

To be compliant, a module must meet at least one complete table in the Memory Timing section of the “PC SGRAM” specification.

2.0 Mechanical Outline

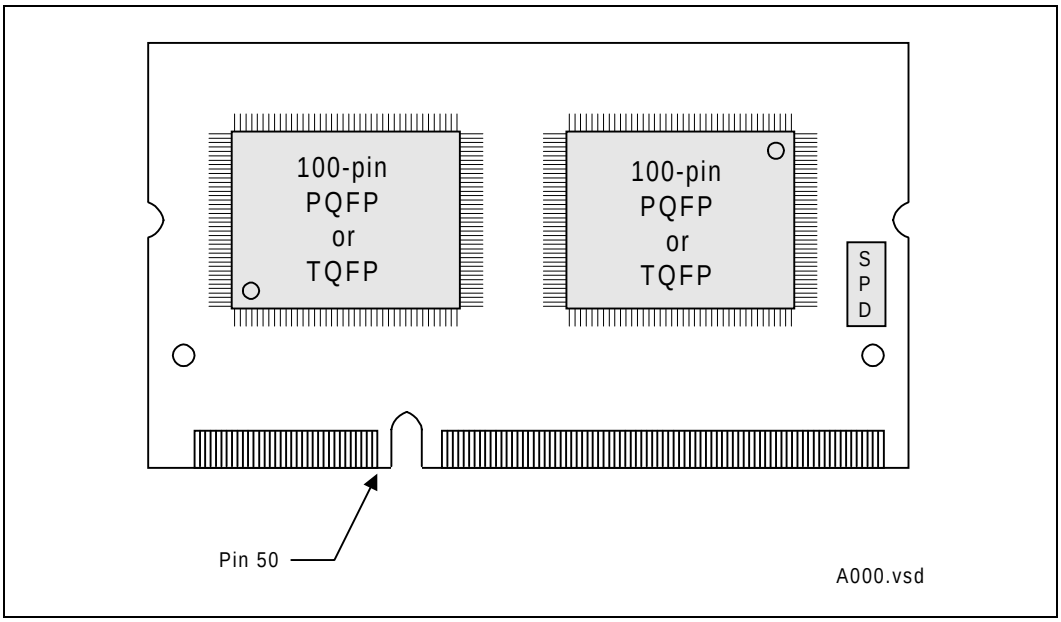
- Dimensions: 67.6 mm (length) X 25.4-50.8 mm (height) X 1.0 mm (thickness)
- 144-pin (0.8 mm pitch zig-zag)

For mechanical specifications of SO-DIMM modules, refer to the JEDEC Committee Ballot

JC-42.5-95-171 144-pin SDRAM SO-DIMM Item 708.4
(herein referred to as the JEDEC SO-DIMM specification).

The key position has been shifted to prevent this module from being inserted into a typical main-memory SDRAM socket.

Figure 1. SDRAM SO-DIMM Module



3.0 Environmental Requirements

Table 1. Environmental Requirements

Operating Temperature	0^{o}C to +65^{o}C
Operating Humidity	10% to 90% relative humidity, noncondensing
Operating Pressure	10.106 PSI (up to 10,000 ft.)
Storage Temperature	-40^{o}C to +70^{o}C
Storage Humidity	5% to 95% without condensation
Storage Pressure	1.682 PSI (up to 50,000 ft.) at 50^{o}C

4.0 Pin Assignments

Table 2. SO-DIMM Module Pin Assignments

PIN #	Front	PIN #	Back	PIN #	Front	PIN #	Back
1	Vss	2	Vss	73	CLK1	74	CLK0
3	DQ63	4	DQ62	75	Vcc	76	Vcc
5	DQ61	6	DQ60	77	RSVD	78	RSVD
7	DQ59	8	DQ58	79	RSVD (A11)	80[1]	A10
9	DQ57	10	DQ56	81[1]	A9	82[1]	A8
11	Vcc	12	Vcc	83	A7	84	A6
13	DQ55	14	DQ54	85	Vss	86	Vss
15	DQ53	16	DQ52	87	A5	88	A4
17	DQ51	18	DQ50	89	A3	90	A2
19	DQ49	20	DQ48	91	A1	92	A0
21	Vss	22	Vss	93	Vcc	94	Vcc
23	DQMB7	24	DQMB6	95	DQ31	96	DQ30
25	DQMB5	26	DQMB4	97	DQ29	98	DQ28
27	Vcc	28	Vcc	99	DQ27	100	DQ26
29	DQ47	30	DQ46	101	DQ25	102	DQ24
31	DQ45	32	DQ44	103	Vss	104	Vss
33	DQ43	34	DQ42	105	DQ23	106	DQ22
35	DQ41	36	DQ40	107	DQ21	108	DQ20
37	Vss	38	Vss	109	DQ19	110	DQ18
39	DQ39	40	DQ38	111	DQ17	112	DQ16
41	DQ37	42	DQ36	113	Vcc	114	Vcc
43	DQ35	44	DQ34	115	DQMB3	116	DQMB2
45	DQ33	46	DQ32	117	DQMB1	118	DQMB0
47	Vcc	48	Vcc	119	Vss	120	Vss
49	RSVD	50	RSVD	121	DQ15	122	DQ14
51	RSVD	52	RSVD	123	DQ13	124	DQ12
53	RSVD	54	RSVD	125	DQ11	126	DQ10
55	Vss	56	Vss	127	DQ9	128	DQ8
57	DSF	58	RFU	129	Vcc	130	Vcc
59	RFU	60	RFU	131	DQ7	132	DQ6
61	RFU	62	SBA	133	DQ5	134	DQ4
63	Vcc	64	Vcc	135	DQ3	136	DQ2
65	CS1	66	CS0	137	DQ1	138	DQ0
67	/RAS	68	/CAS	139	Vss	140	Vss
69	/WE	70	CKE	141	SDA	142	SCL
71	Vss	72	Vss	143	Vcc	144	Vcc

NOTE:
1. Refer to Table 3 “Address Translation” on page 9 for determining SO-DIMM to SGRAM device (256Kx32 or 512Kx32) connections for pins 80, 81 and 82.

5.0 Graphics SO-DIMM Block Diagram

Figure 2 through Figure 5 illustrate the electrical connectivity of several SO-DIMM configurations. The series termination resistors on CLK0 and CLK1 are not currently used and should be set to 0 ohms. Table 3 “Address Translation” on page 9 should be followed for connecting 256Kx32 and 512Kx32 devices.

Figure 2. 256K/512 x 64 SGRAM SO-DIMM Block Diagram (1 bank of two 256K/512K x 32)

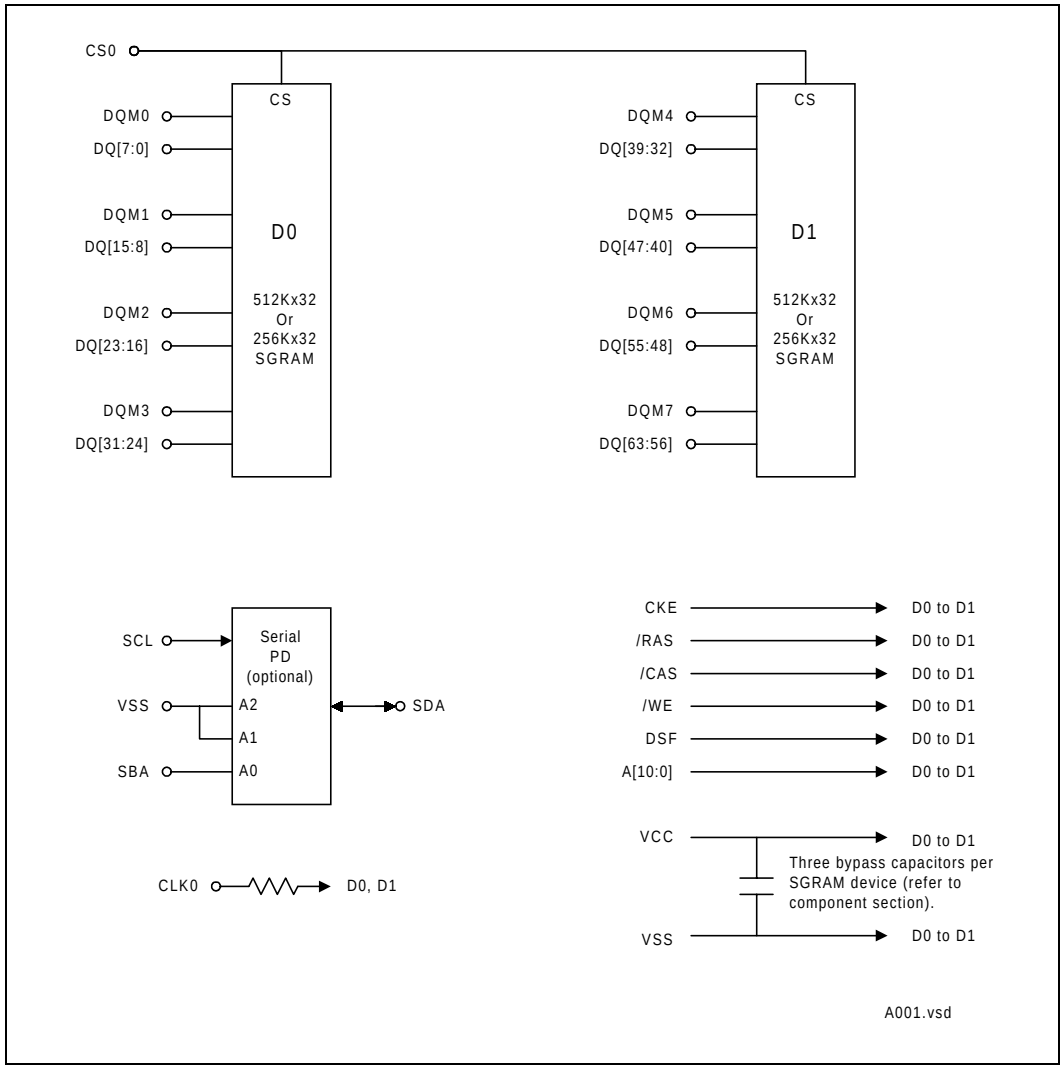


Figure 3. 512K/1M x 64 SGRAM SO-DIMM Block Diagram (2 banks of two 256K/512K x 32)

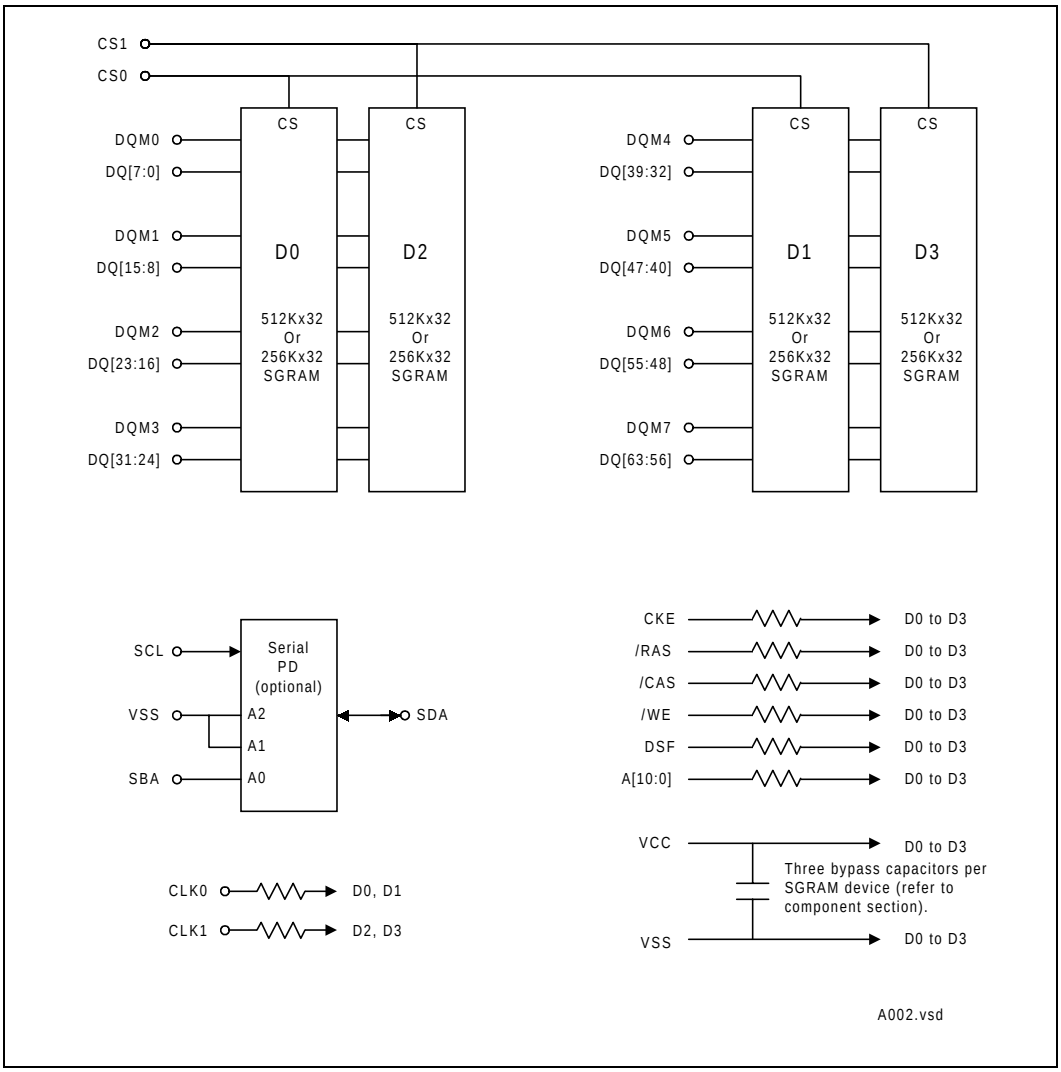


Figure 4. 256K/512K x 32 SGRAM SO-DIMM Block Diagram (1 bank of one 256K/512K x 32)

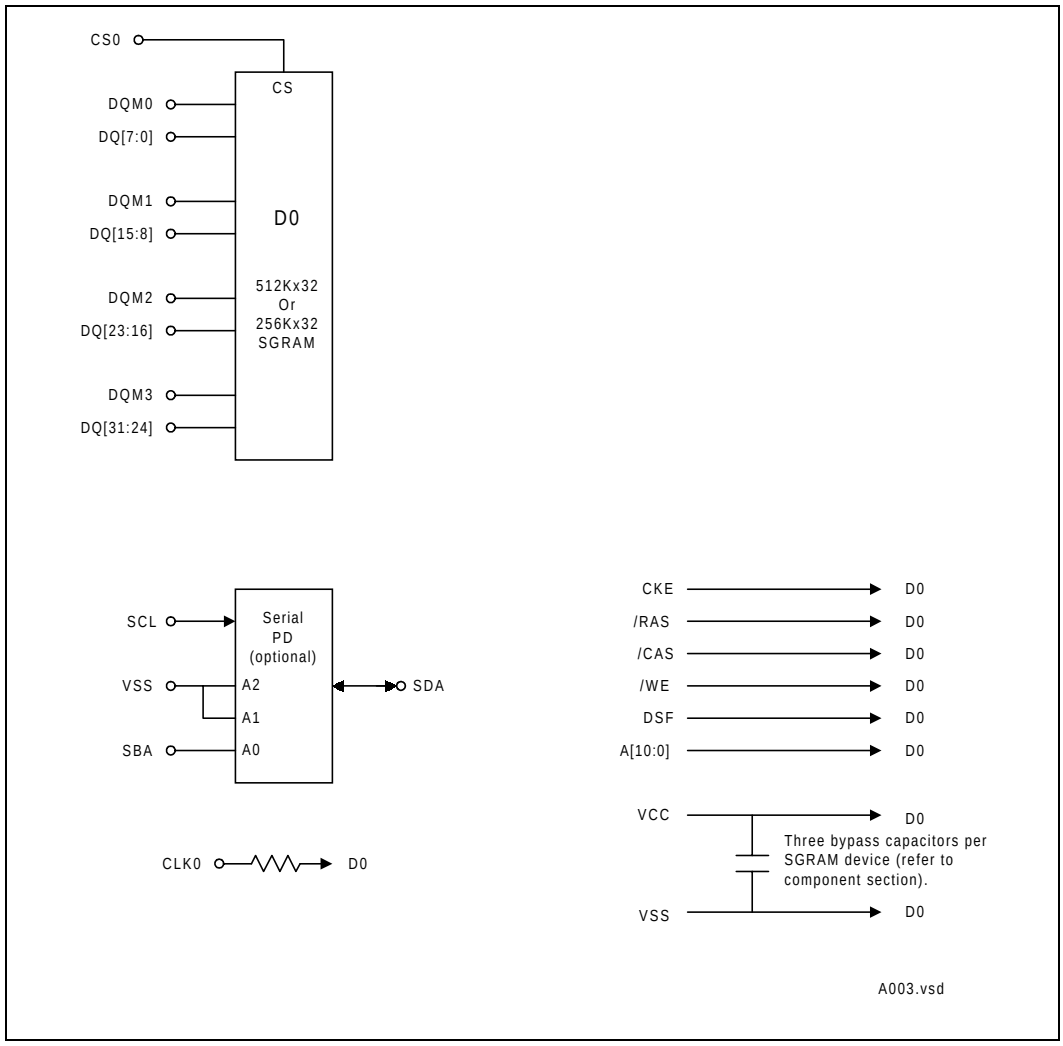
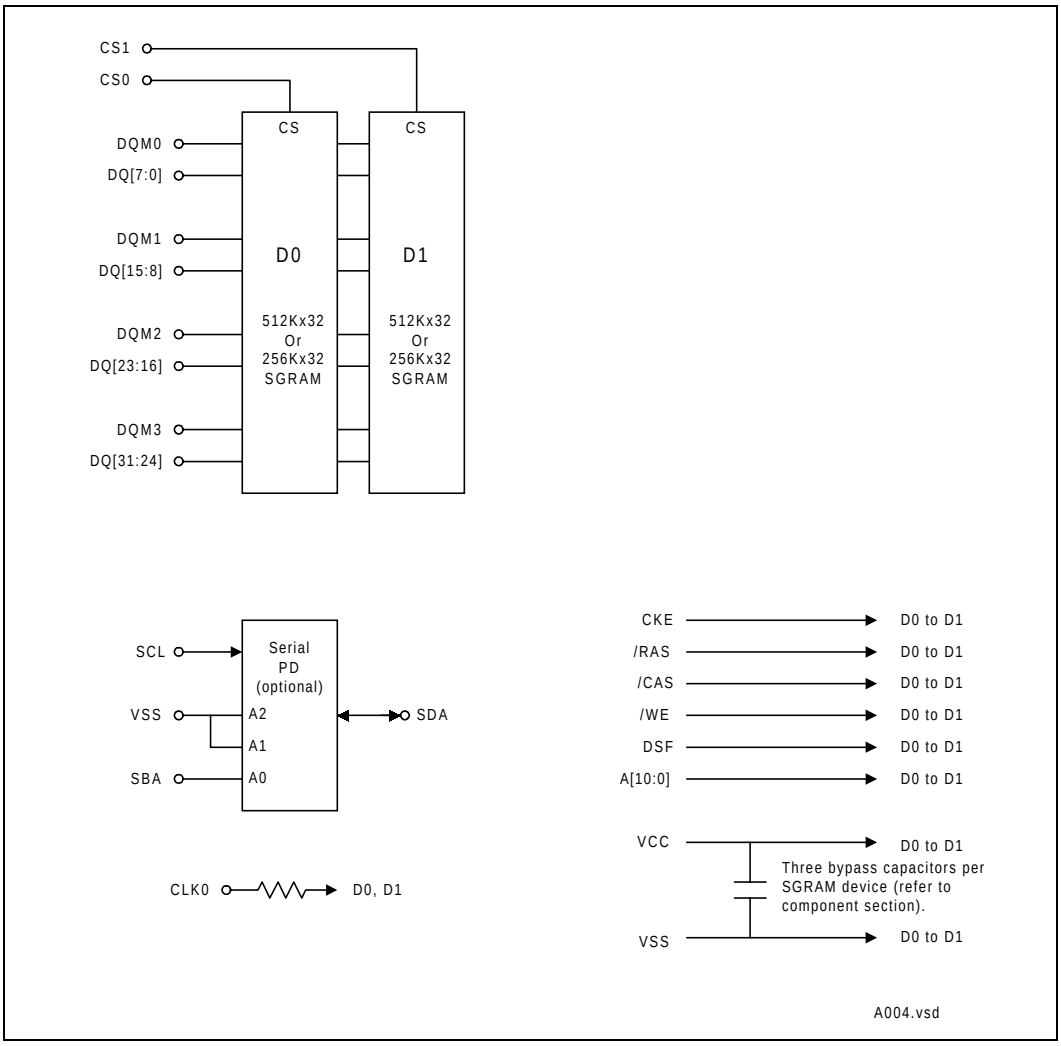


Figure 5. 512K/1M x 32 SGRAM SO-DIMM Block Diagram (2 banks of one 256K/512K x 32)



6.0 Address Translation

Table 3 should be followed for 256Kx32 and 512Kx32 SGRAM devices. This table specifies the SGRAM device to SO-DIMM connector connections for a 256Kx32 and 512Kx32 devices.

Table 3. Address Translation

SODIMM		256Kx32		512Kx32	
Pin #	Functionality	Pin #	Functionality	Pin #	Functionality
92	A0	31	A0	31	A0
91	A1	32	A1	32	A1
90	A2	33	A2	33	A2
89	A3	34	A3	34	A3
88	A4	47	A4	47	A4
87	A5	48	A5	48	A5
84	A6	49	A6	49	A6
83	A7	50	A7	50	A7
82	A8	51	A8/AP	51	A9/AP
81	A9	29	A9/BA	29	A10/BA
80	A10	No Connect	No Connect	30	A8
79	A11/Reserved	No Connect	No Connect	No Connect	No Connect

NOTES:
1. The names for pin 80, 81 and 82 are different for 256Kx32 and 512Kx32 device connection.
2. SO-DIMM's pin 80 (which is labeled as A10) is a no connect for 256Kx32 device and is connected to pin 30 (labeled as A8) of 512Kx32 device.
3. SO-DIMM's pin 81 (which is labeled as A9) is connected to pin 29 (labeled as A9/BA) of 256Kx32 device and is connected to pin 29 (labeled as A10/BA) of 512Kx32 device
4. SO-DIMM's pin 82 (which is labeled as A8) is connected to pin 51 (labeled as A8/BA) of 256Kx32 device and is connected to pin 51 (labeled as A9/AP) of 512Kx32 device.

6.1 Configuration

Graphic controllers can determine the module capabilities one of three ways; they are:

- Using the default parameters with power-up testing
- Using resistor strapping options on the data lines
- Using an optional Serial Presence Detect EEPROM

Modules are required to include resistor support (3 resistors); the Serial Presence Detect EEPROM is optional.

6.2 Default Parameters

All memory modules must meets these baseline component requirements.

Table 4. Module Baseline Component Requirements

Parameter	Min.	Max.	Unit	Notes
Clock Period	15.0		nS	
Clock High Time	5.0		nS	Rated @ 1.4V
Clock Low Time	5.0		nS	
DQM#/CS# Input Setup Time	3.0		nS	
Other Input Setup Time	3.0		nS	
DQM#/CS# Input Hold Time	1.0		nS	
Other Input Hold Time	1.0		nS	
Output Valid from Clock		11.0	nS	Rated @ 30pf
Output Hold from Clock	2.5		nS	Rated @ 30pf
CAS Latency	2	2	Tclk	
CAS to CAS Delay	1		Tclk	
CAS Bank Delay	1		Tclk	
CKE to Clock Disable	1	1	Tclk	
RAS Precharge Time	3		Tclk	
RAS Active Time	4		Tclk	
Activate to Command Delay (RAS to CAS Delay)	2		Tclk	
RAS to RAS Bank Activate Delay	2		Tclk	
RAS Cycle Time	7		Tclk	
DQM to Input Data Delay	0	0	Tclk	
Write Cmd. to Input Data Delay	0	0	Tclk	
Mode Register set to Active delay	3		Tclk	
Precharge to O/P in High-Z	2		Tclk	
DQM to Data in HiZ for read	2	2	Tclk	
Data in to Precharge	2		Tclk	
Data in to Activate/Refresh	5		Tclk	
DQM to Data mask for write	0	0	Tclk	
Number of Banks per SDRAM/SGRAM device	2	2	Banks	

Module should follow the AC timings specified in the “PC SGRAM” specification.

The graphic controller must assume that the memory is SDRAM unless it can determine that SGRAM functions (block write and write-per-bit) are available. This can be done at power-up using the DSF pin. Modules which do not support SGRAM special functions must disable the DSF pin.

The graphic device must determine the data width of the module, number of row addresses, and number of column addresses.

6.3 Resistor Strapping Options

Three resistor straps are used to indicate the synchronous clock frequency (period) and memory timing. Timing information for each clock frequency is indicated in the section titled *Memory Timing*. Memory modules must meet all timing requirements within the specified operating environment.

6.3.1 Clock Frequency and Memory Timing

Cycle Time	DQ30	DQ29
15 nS	0	0
12 nS	0	1
10 nS	1	0
8 nS	1	1

6.3.2 CAS Latency

CAS Latency	DQ31
3	0
2 and 3	1

A logic low (0) indicates that the resistor strapping is tied to ground (Vss). A logic high (1) indicates that the resistor strapping is tied to Vcc. Resistors should be a 4.7 Kohm resistor on the DQ lines.

6.4 Serial Presence Detect EEPROM

This EEPROM is optional on the module. For additional information, refer to the Intel document *66 MHz Unbuffered SDRAM SO-DIMM Specification*.

7.0 Electrical Characteristics

The module electrical characteristics are carefully controlled to allow system configurations with two separate memory arrays. This allows one module to be present, plus memory soldered directly to the motherboard or add-in card PCB. Currently, two modules are not being supported. Routing on the main board will generally be done as a T-topology. The module's electrical characteristics (as well as the main board's characteristics) must be carefully implemented to insure a balanced T-topology.

The board must have a characteristic impedance between 50 and 85 ohms.

The following table lists the suggested flight time budgets for a typical graphic system using an early/late memory clock.

7.1 15 nS Timing

Parameter	Symbol	Min.	Max.	Unit
Clock Cycle Time	Tcyc	15.0		nS
Early/Late Clock	Tcsk	0.35	1.6	nS
Output Valid from Clock	Tac		11.0	nS
Output Hold from Clock	Toh	2.5		nS
Input Setup Time	Tsi	3.0		nS
Input Hold Time	Thi	1.0		nS
Motherboard Clock Flight Time	Tcfm	0	0.3	nS
Motherboard Addr/Data/Cntrl Flight Time	Txfm	0	0.3	nS
Module Clock Flight Time	Tcfs	0.1	0.365	nS
Module Flight Addr/Data/Cntrl Flight Time	Txfs	0	0.375	nS

7.2 12 nS Timing

Parameter	Symbol	Min.	Max.	Unit
Clock Cycle Time	Tcyc	12.0		nS
Early/Late Clock	Tcsk	1.3	1.8	nS
Output Valid from Clock	Tac		9.0	nS
Output Hold from Clock	Toh	2.5		nS
Input Setup Time	Tsi	3.0		nS
Input Hold Time	Thi	1.0		nS
Motherboard Clock Flight Time	Tcfm	0.2	0.3	nS
Motherboard Addr/Data/Cntrl Flight Time	Txfm	0	0.3	nS
Module Clock Flight Time	Tcfs	0.175	0.325	nS
Module Flight Addr/Data/Cntrl Flight Time	Txfs	0	0.375	nS

7.3 10 nS Timing

Parameter	Symbol	Min.	Max.	Unit
Clock Cycle Time	Tcyc	10.0		nS
Early/Late Clock	Tcsk	1.3	1.8	nS
Output Valid from Clock	Tac		7.0	nS
Output Hold from Clock	Toh	2.5		nS
Input Setup Time	Tsi	2.5		nS
Input Hold Time	Thi	1.0		nS
Motherboard Clock Flight Time	Tcfm	0.2	0.3	nS
Motherboard Addr/Data/Cntrl Flight Time	Txfm	0	0.3	nS
Module Clock Flight Time	Tcfs	0.175	0.325	nS
Module Flight Addr/Data/Cntrl Flight Time	Txfs	0	0.375	nS

7.4 8 nS Timing

Parameter	Symbol	Min.	Max.	Unit
Clock Cycle Time	Tcyc	8.0		nS
Early/Late Clock	Tcsk	1.3	1.8	nS
Output Valid from Clock	Tac		6.0	nS
Output Hold from Clock	Toh	2.5		nS
Input Setup Time	Tsi	2.0		nS
Input Hold Time	Thi	1.0		nS
Motherboard Clock Flight Time	Tcfm	0.2	0.3	nS
Motherboard Addr/Data/Cntrl Flight Time	Txfm	0	0.3	nS
Module Clock Flight Time	Tcfs	0.175	0.325	nS
Module Flight Addr/Data/Cntrl Flight Time	Txfs	0	0.375	nS

7.5 A.C Timing Diagrams

Figure 6. Address/Control A.C. Timing Parameters

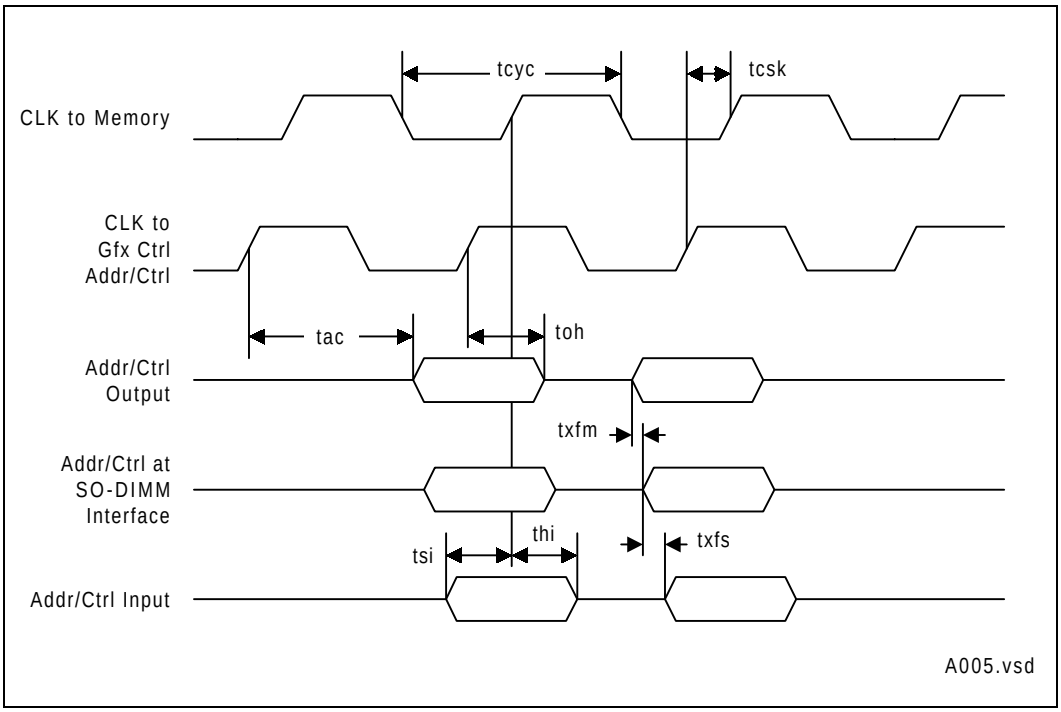


Figure 7. Data Write A.C. Timing Parameters

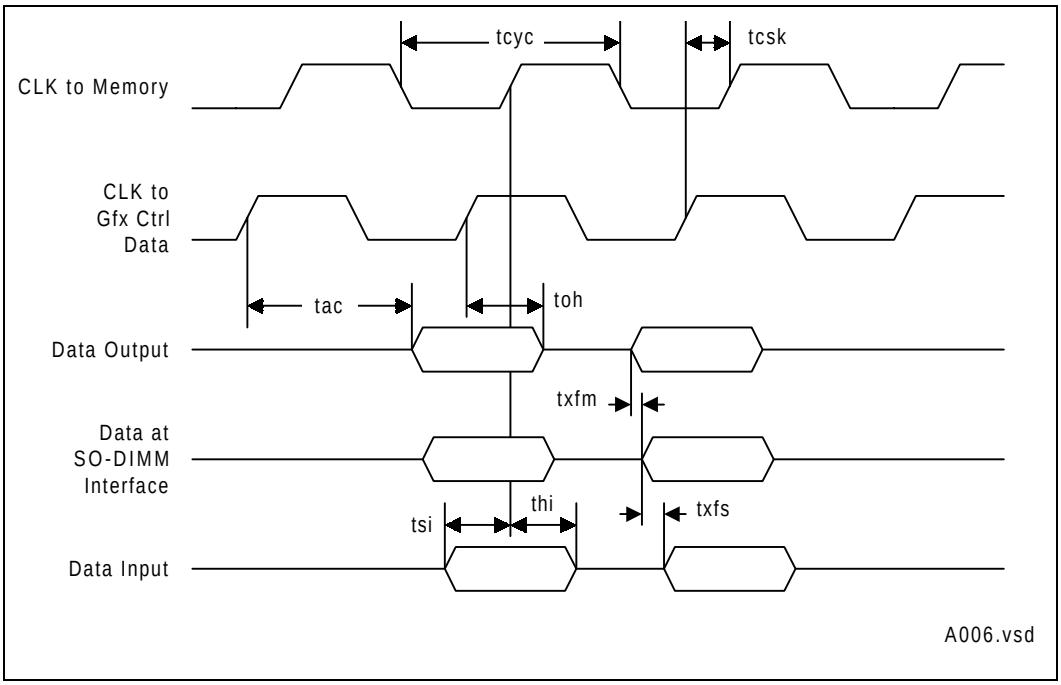
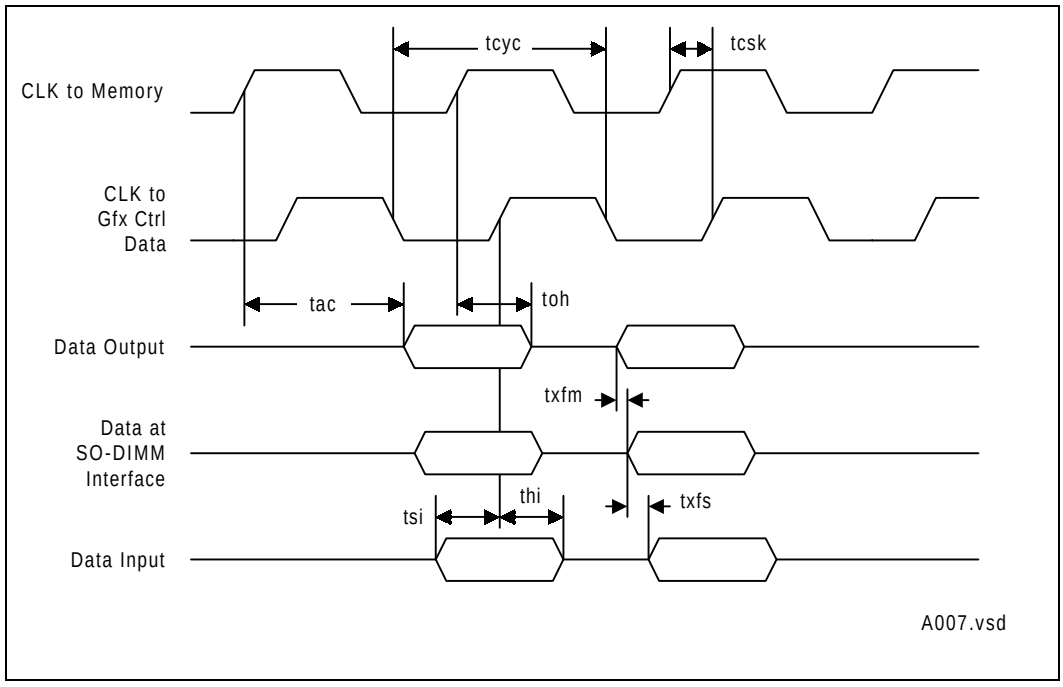


Figure 8. Data Read A.C. Timing Paramters



8.0 PCB Layout Considerations

To insure proper signal integrity, the module routing must be taken under careful considerations. This section outlines PCB layout considerations for the SO-DIMM module.

Each section looks at three separate topologies; one for clocks, one for control/address, and one for data. The assumed loading for this configuration is:

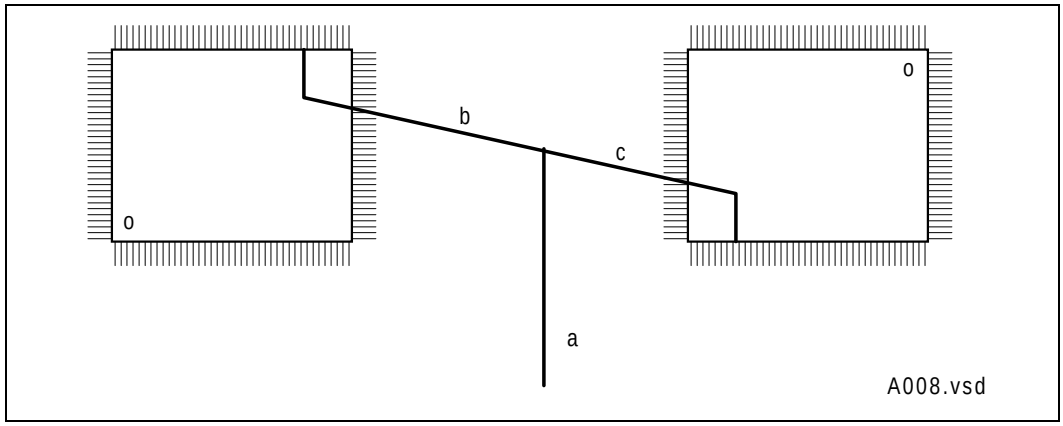
Table 5. Signal Loading

Signal	32-bit		64-bit	
	Single-sided	Double-sided	Single-sided	Double-sided
clocks	1 load	1 load	2 loads	2 loads
address/control	1 load	2 loads	2 loads	4 loads
data	1 load	2 loads	1 load	2 loads

8.1 Clock Routing and Chip Selects

Clock and chip select loading is two loads per line, maximum. Routing should be performed using a T-topology, as shown below:

Figure 9. T-Topology Clock Routing



The following table lists the allowable stub lengths for the clock and chip select routing.

Table 6. Stub Lengths (Clock and Chip Select Routing)

Parameters	SDRAM/SGRAM Clock Frequency								Units
	15 nS		12 nS		10 nS		8 nS		
	Min.	Max	Min.	Max	Min.	Max	Min.	Max	
a	75	150	75	150	75	150	75	150	pS
b	0	115	0	115	0	115	0	115	pS
c	0	115	0	115	0	115	0	115	pS
b+c	0	225	0	225	0	225	0	225	pS
Total Length (clock)	100	365	175	325	175	325	175	325	pS
Total Length (chip select)	0	365	0	365	0	365	0	365	pS

8.2 Address/Control Routing

The following table lists the allowable stub lengths for the address/control routing.

Figure 10. Address and Control Routing

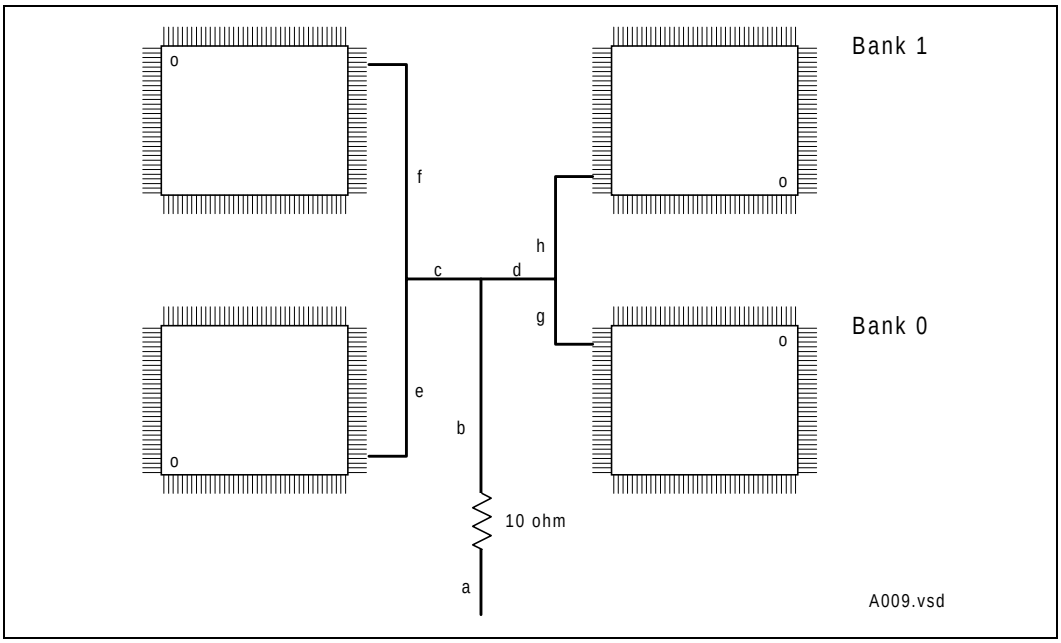


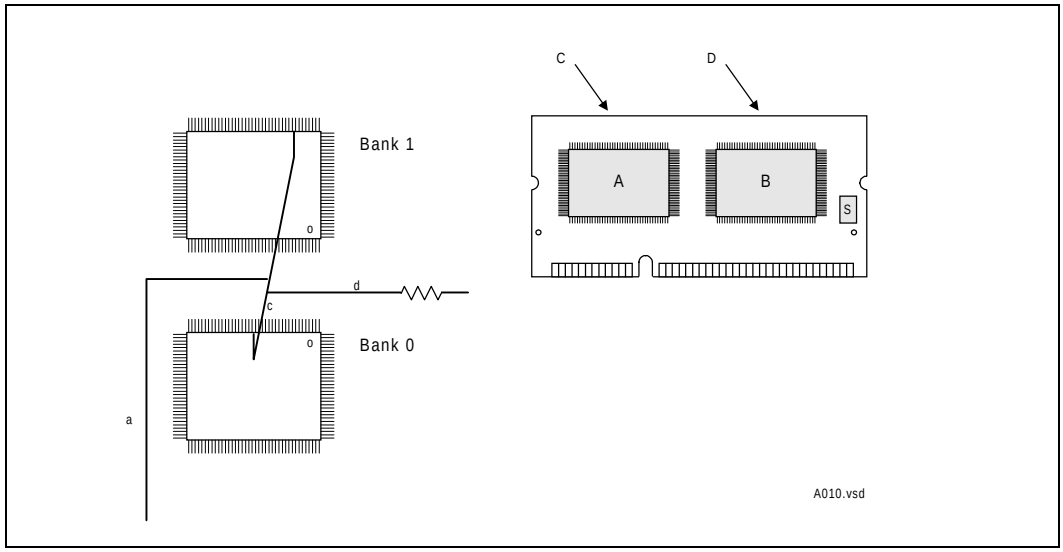
Table 7. Stub Lengths (Address/Control Routing)

Parameters	SDRAM/SGRAM Clock Frequency								Units
	15 nS		12 nS		10 nS		8 nS		
	Min.	Max	Min.	Max	Min.	Max	Min.	Max	
a	0	37	0	37	0	37	0	37	pS
b	0	190	0	190	0	190	0	190	pS
c	0	115	0	115	0	115	0	115	pS
d	0	115	0	115	0	115	0	115	pS
e	0	115	0	115	0	115	0	115	pS
f	0	115	0	115	0	115	0	115	pS
g	0	115	0	115	0	115	0	115	pS
h	0	115	0	115	0	115	0	115	pS
b-c	-75	75	-75	75	-75	75	-75	75	pS
b-d	-75	75	-75	75	-75	75	-75	75	pS
c+e	0	190	0	190	0	190	0	190	pS
c+f	0	190	0	190	0	190	0	190	pS
d+g	0	190	0	190	0	190	0	190	pS
d+h	0	190	0	190	0	190	0	190	pS
total length	0	375	0	375	0	375	0	375	pS

8.3 Data Routing

Data lodading is two loads per line, maximum. Routing should be performed using a T-topology, as shown below.

Figure 11.Data Routing



Byte-ordering (along with the respective Data Mask, DQM) within the SDRAM/SGRAM should be swapped to optimize routing.

Table 8. Byte Ordering

Module Byte	Front-Side Memory Byte	Back-Side Memory Byte	*n* value
BYTE 0	Memory B; BYTE 0	Memory D; BYTE 3	*n* = 115 pS
BYTE 1	Memory B; BYTE 3	Memory D; BYTE 0	*n* = 35 pS
BYTE 2	Memory B; BYTE 1	Memory D; BYTE 2	*n* = 35 pS
BYTE 3	Memory B; BYTE 2	Memory D; BYTE 1	*n* = 115 pS
BYTE 4	Memory A; BYTE 1	Memory C; BYTE 2	*n* = 115 pS
BYTE 5	Memory A; BYTE 2	Memory C; BYTE 1	*n* = 35 pS
BYTE 6	Memory A; BYTE 0	Memory C; BYTE 3	*n* = 35 pS
BYTE 7	Memory A; BYTE 3	Memory C; BYTE 0	*n* = 115 pS

The following table lists the allowable stub lengths for the data line routing.

Table 9. Stub Lengths (Data Line Routing)

Parameters	SDRAM/SGRAM Clock Frequency								Units
	15 nS		12 nS		10 nS		8 nS		
	Min.	Max	Min.	Max	Min.	Max	Min.	Max	
a	n	n+75	n	n+75	n	n+75	n	n+75	pS
b	0	75	0	75	0	75	0	75	pS
c	0	75	0	75	0	75	0	75	pS
d	0	125	0	125	0	125	0	125	pS
total length	0	n+150	0	n+150	0	n+150	0	n+150	pS

Stub *d* is used for the strapping resistors on DQ29-DQ31, and is optional.

9.0 Electrical Specifications

The following information is from the Intel *PC SDRAM* Specification, version 1.1, April 1996. It is provided here for convenience

9.1 SDRAM/SGRAM Component Absolute Maximum D.C. Ratings

Table 10. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
Vin, Vout	Voltage on any pin w.r.t V_{SS}	-0.5	VCC + 0.5	V
VCC, VCC_Q	Voltage Supply pins w.r.t V_{SS}	-0.5	4.5	V
Ts	Storage Temperature	-55	125	°C
PD	Power Dissipation		1	W

9.2 SDRAM/SGRAM Components D.C. Operating Requirements

Table 11. D.C. Operating Requirements

Symbol	Parameter	Condition	Min.	Max.	Units	Notes
VCC	Supply Voltage		3.0	3.6	V	
VCCQ	I/O Supply Voltage		3. 0	3.6	V	
Iil	Input Leakage Current	0 < Vin < VCCQ	-5	+5	µA	1,2
Voh	Output High Voltage	Ioh = -4 mA	2.4		V	
Vol	Output Low Voltage	Iol = 4 mA		0.4	V	
Cin	Input/Clock Pin Capacitance			5	pF	
CI/O	I/O Pin Capacitance			7	pF	
Lpin	Pin Inductance			10	nH	2
Ta	Ambient Temperature	No Airflow	0	65	°C	

NOTES:
1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
2. This is a recommendation, not an absolute requirement. The actual value should be provided with the component data sheet.

9.3 SDRAM/SGRAM Components Absolute Maximum A.C. Operating Requirements

Table 12. Absolute Maximum A.C. Operating Requirements

Symbol	Parameter	Min.	Max.	Units	Notes
Vih	Input High Voltage	2.0	VCCQ + 1.5	V	1
Vil	Input Low Voltage	VSSQ – 1.5	0.8	V	1

NOTE: The overshoot and undershoot voltage duration is ≤5ns with no input clamp diodes.

9.4 Memory Timing

Individual DRAM component devices are required to follow the AC timings specified in the Intel “PC SGRAM” specification. Devices which can not meet the minimum timing set forth. must program a lower clock speed.

Appendix A PCB Layout

This section show an example of a PQFP/TQFP SO-DIMM module routed as a six-layer PCB.

Figure 12.Silk Screen - Primary Side

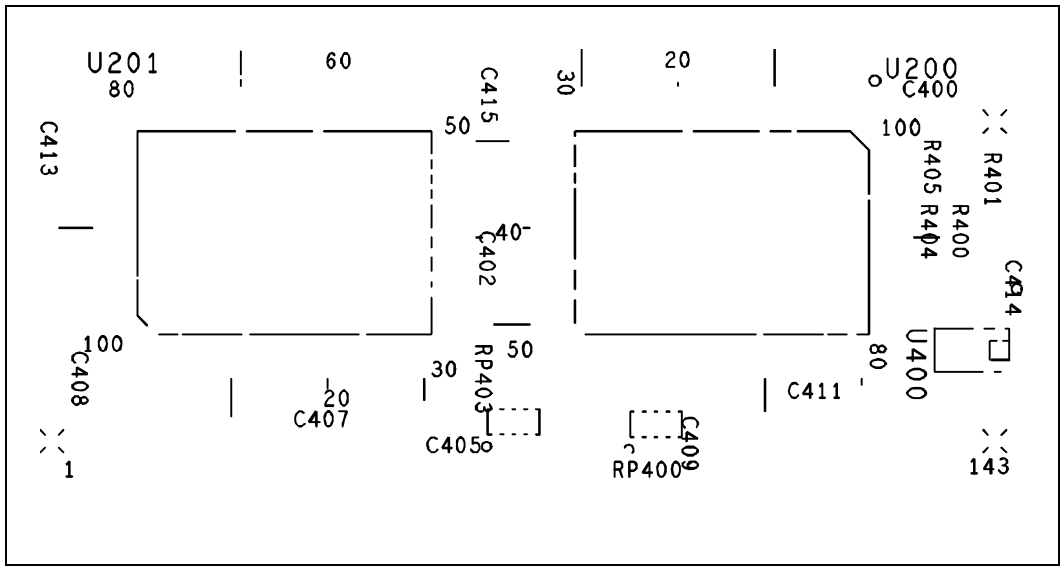


Figure 13.Silk Screen - Secondary Side

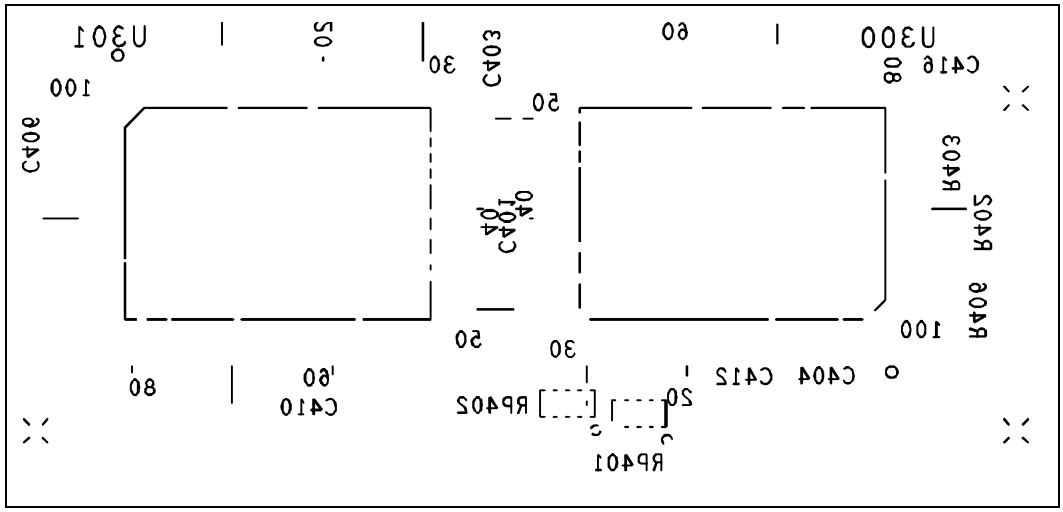


Figure 14.Primary Side (layer 1)

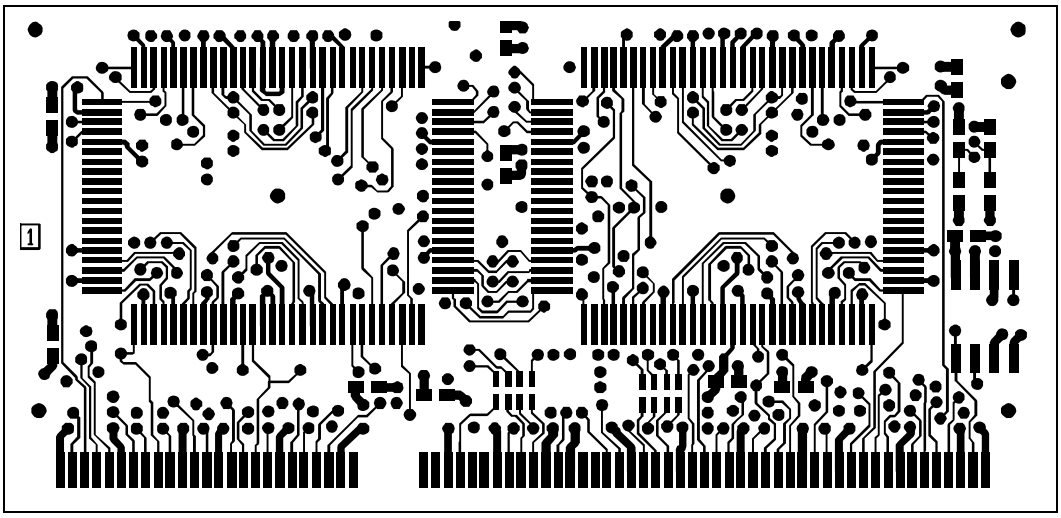


Figure 15.VCC Plane (layer 2)

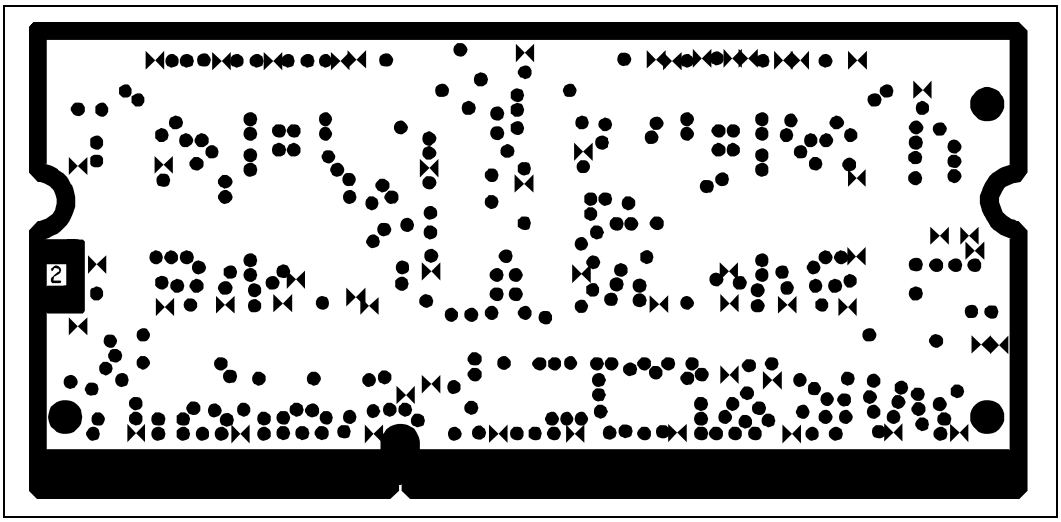


Figure 16.Inner-Signal (layer 3)

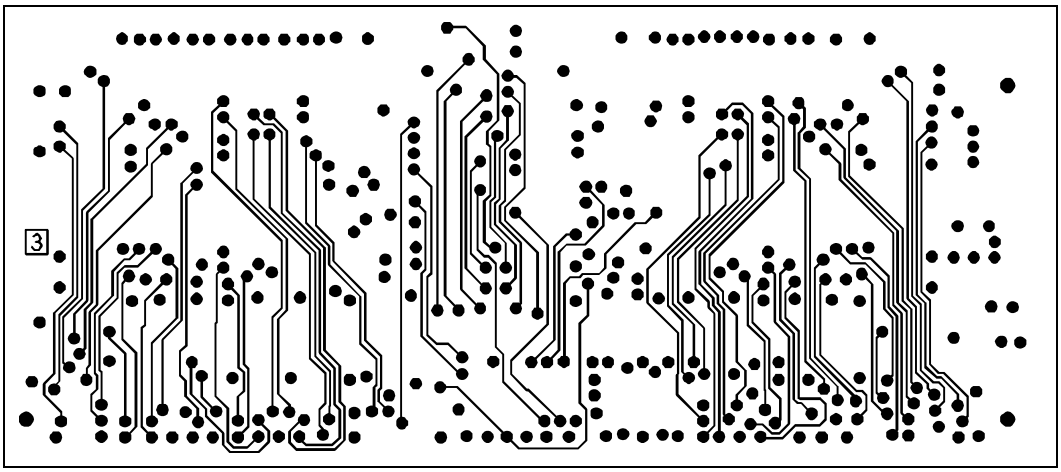


Figure 17.Inner-Signal (layer 4)

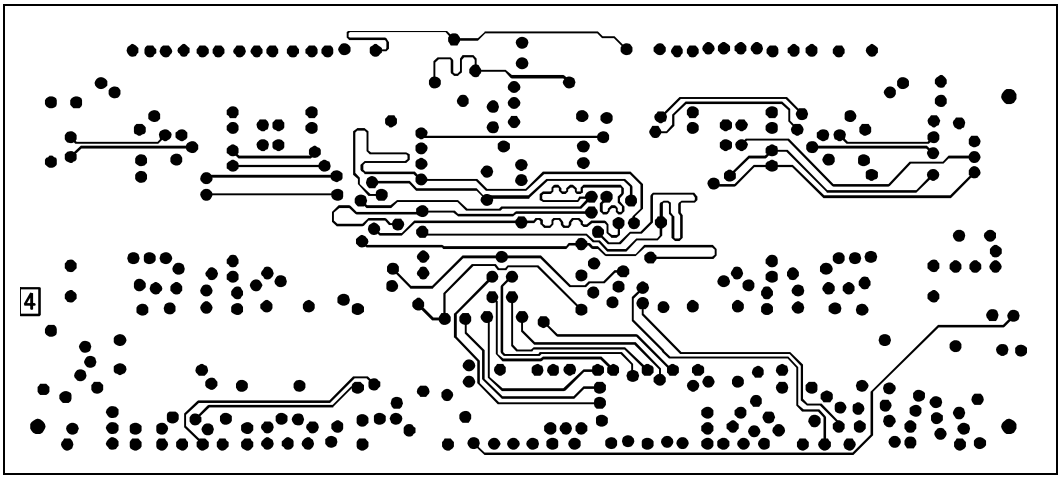


Figure 18.Ground Plane (layer 5)



Figure 19.Secondary Side (layer 6)

